Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A motherboard comprising:
at least a first memory slot;
at least a second memory slot; and
a single-channel memory controller electrically connected to the first memory slot and the second memory slot through a first bus and a second bus.

[c2] 2. The motherboard of claim 1 wherein each of the first and second buses is used for transferring memory data, memory addresses, and control signals.

[c3] 3. The motherboard of claim 1 wherein the single-channel memory controller comprises:
a memory data input/output port for outputting a memory data to the first and second memory slots through the first and second buses;
a memory address output port for outputting a memory address to the first and second memory slots through the first and second buses; and
a control signal output port for outputting a control signal to the first and second memory slots through the first and second buses.

[c4] 4. The motherboard of claim 1 wherein the single-channel memory controller is positioned inside a package, and the package comprises:
at least two first external contacts connected to the first and second buses respectively for transferring memory data;
at least two second external contacts connected to the first and second buses respectively for transferring memory addresses;
at least two third external contacts connected to the first and second buses respectively for transferring control signals; and
a plurality of traces electrically connected to the first external contacts and a memory data input/output port of the single-channel memory controller, electrically connected to the second external contacts and a memory address output port of the single-channel memory controller, and electrically connected to the third external contacts and a control signal output port of the single-channel memory controller.

[c5] 5. A computer system comprising:
at least a first dynamic random access memory;
at least a second dynamic random access memory; and
a single-channel memory controller connected to a first bus and a second bus respectively for controlling the

first dynamic random access memory and the second dynamic random access memory.

[c6] 6. The computer system of claim 5 wherein each of the first and second buses is used for transferring memory data, memory addresses, and control signals.

[c7] 7. The computer system of claim 5 wherein the single-channel memory controller comprises:
a memory data input/output port for outputting memory data to the first and second memory slots through the first and second buses;
a memory address output port for outputting memory addresses to the first and second memory slots through the first and second buses; and
a control signal output port for outputting control signals to the first and second memory slots through the first and second buses.

[c8] 8. The computer system of claim 5 wherein the single-channel memory controller is positioned inside a package, and the package comprises:
at least two first external contacts connected to the first and second buses respectively for transferring memory data;
at least two second external contacts connected to the first and second buses respectively for transferring

memory addresses;

at least two third external contacts connected to the first and second buses respectively for transferring control signals; and

a plurality of traces electrically connected to the first external contacts and a memory data input/output port of the single-channel memory controller, electrically connected to the second external contacts and a memory address output port of the single-channel memory controller, and electrically connected to the third external contacts and a control signal output port of the single-channel memory controller.

[c9] 9. A package comprising:

a single-channel memory controller;

a plurality of first external contacts electrically connected to a memory data input/output port, a memory address output port, and a control signal output port of the single-channel memory controller, the first external contacts being used for connecting a first memory bus; and

a plurality of second external contacts electrically connected to the memory data input/output port, the memory address output port, and the control signal output, the second external contacts being used for connecting a second memory bus.

[c10] 10. The package of claim 9 wherein the first memory bus is used for controlling a first memory slot, and the second memory bus is used for controlling a second memory slot.

[c11] 11. The package of claim 9 wherein the first memory bus is used for controlling a first dynamic random access memory, and the second memory bus is used for controlling a second dynamic random access memory.